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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/411,917	10/04/1999	NAOMI YAMAZAKI	FUJO-16.572	8953

7590 10/22/2002

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EXAMINER
TRAN, THIEN D

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/411,917	YAMAZAKI, NAOMI	
	Examiner	Art Unit	
	Thien D Tran	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishihara et al (U.S Patent No 6,021,135).

Regarding claim 1, Ishihara discloses a cross-connection switch comprising:

management memory table 27 (first memory means) for storing data indicating switching information of a time slot at an address to which time slot information is assigned (col.9 line 56);

memory 25 (second memory means) for storing data of each time slot of an input frame in time slot units, inputting data stored in said first memory means, and outputting

the data stored at the address specified by the data as time slot data of an output frame (col.9 lines 35-40, 54); and

counter means for counting a number of input time slots of an input frame, and outputting the count value as a read address and a write address respectively to said first memory means and said second memory means. See col.9 lines 50-65, col.10 lines 30-40).

Regarding claim 2, Ishihara discloses a multiplexed line signal having an input frame of n bits per channel is processed, a time slot number of each bit of an n-bit channel is assigned to addresses of said first memory means, and data indicating switching information about a time slot of each piece of bit data is entered at each address of said second memory means. See col.14 lines 30-40, col.9 lines 40-65.

Regarding claim 3, Ishihara discloses a plurality of lines are accommodated by said cross-connection switch, any line of the plurality of lines is selected for a switching process by entering switching information about time order of data of a time slot and switching information data between lines at each address of said first memory means. See col.7 lines 15-35.

Regarding claim 4, Ishihara discloses that information of a current input time slot is written to said second memory means, data to be used in processing one time slot before the current input time slot is read from said first memory means, a read address is output from said first memory means to said second memory means, and time slot data used in processing the one time slot before the current input time slot is read from said second memory means. See col.10 lines 25-45.

Regarding claim 5, Ishihara discloses that selector means for switching data of a time slot directly input from an input line with data of a time slot read from said second memory means and outputting a switching result, wherein said selector means is controlled to output time slot information not to be switched as time slot data of an output frame without performing a process on the information by inputting information read from said first memory means as a selector signal to said selector means, and to output time slot data read from said second memory means as time slot data of an output frame to be switched. See col.8 lines 25-50.

Regarding claim 6, Ishihara discloses that flip-flop means for holding data of a time slot read from said second memory means, wherein a timing of a switching process of said selector means is adjusted by inputting to said flip-flop means a second clock generated by adjusting a phase of a first clock synchronous with a time slot of an input frame by inputting to said flip-flop means time slot data used as data of one time slot earlier than a current point from said second memory means. See col.13 lines 35-60.

Regarding claim 7, Ishihara discloses that phase adjustment means for inputting the first clock, and generating the second clock whose phase is faster than the first clock by a predetermined time with an output delay of said flip-flop means and a switching delay of said selector means taken into account, wherein said output delay and said switching delay are absorbed by inputting the second clock generated by said phase adjustment means as a clock signal to said flip-flop means. See col.12 lines 5-60.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Tsui et al (US Patent No. 6,347,089 B1) discloses simplified ethernet frame switching system architecture without local buffer requirement.

-Sindhu et al (US Patent No. 5,905,725) discloses high speed switching device.

-Lincoln (US Patent No. 5,991,265) discloses asynchronous transfer mode system and method.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4388. The examiner can normally be reached on Monday-Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (703) 308-6602. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Thien Tran

ALPUS H. HSU
PRIMARY EXAMINER